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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,384	06/21/2000	Yasuaki Hirano	204552018400	6872

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EXAMINER	
PHAN, TRONG Q	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/598,384	Applicant(s) HIRANO, YASUAKI	
	Examiner TRONG PHAN	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Drawings

1. Figures 19 and 21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: hrdab, O, hrdab and 31 in Fig. 3; hnset and erssetupb in Fig. 4; hhvpre, hnvpnx, hnvneg, hnset, n1, n2, P3, P4, and N7-N11 in Fig. 5; erssetup, sel0, hners, hnn0, n3, P5-P6 and N13-N14 in Fig. 6; three NAND gates and NOR gate in Fig. 7; four NAND gates, two inverters and NOR gate in Fig. 8; detailed elements in Figs. 9B, 9C, 9E, 9F, 9G, 9H, 9I, 9J and 9L; detailed elements in Figs. 10B to 10L; detailed elements in Figs. 11A to 11M; PCONTROL CIRCUIT 0 to 31, hrdab, O, hrdab, and 31 in Fig. 12; prgsetup, hnset, n5, erssetupb, N21-N24, exclusive gate, two NAND gates and four transistors in latch circuit B in Fig. 13; wlon, prgsetup, hhvpp, n6-n7, P11-P12, N25-N26, two NAND gates, three inverters and two output transistors in Fig. 14; all elements except hnn0 in Fig. 15; all detailed elements in Figs. 16A-16O; all detailed elements in Figs. 17A-17O; all detailed elements in Figs. 18A-18Q. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

`Arrangement of the Specification`

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT:
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The BRIEF SUMMARY OF THE INVENTION is not included.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

4. Claims 3-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 3-6 are rejected for claiming the invention which does not contain subject matter complying with the enablement requirement as follows:

a) it is not understood what the following elements, hnset and erssetupb in Fig. 4; hhvpre, hnvpnx, hnvneg, hnset, n1, n2, P3, P4, and N7-N11 in Fig. 5; erssetup, sel0, hners, hnn0, n3, P5-P6 and N13-N14 in Fig. 6; three NAND gates and NOR gate in Fig. 7; four NAND gates, two inverters and NOR gate in Fig. 8; detailed elements in Figs. 9B, 9C, 9E, 9F, 9G, 9H, 9I, 9J and 9L; detailed elements in Figs. 10B to 10L; detailed elements in Figs. 11A to 11M; PCONTROL CIRCUIT 0 to 31 in Fig. 12; prgsetup, hnset, n5, erssetupb, N21-N24, exclusive gate, two NAND gates and four transistors in latch circuit B in Fig. 13; wlon, prgsetup, hhvpp, n6-n7, P11-P12, N25-N26, two NAND gates, three inverters and two output transistors in Fig. 14; all elements except hnn0 in Fig. 15; all detailed elements in Figs. 16A-16O; all detailed elements in Figs. 17A-17O; and all detailed elements in Figs. 18A-18Q, really are since they are not described in the specification;

b) it is not understood how each of the P-channel transistors and the N-channel transistors, as described in lines 3-25, page 28; lines 1-23, page 29; lines 6-13, page 32; lines 19-25, page 54; lines 1-25, page 55; lines 20-21, page 60; lines 11-13, page 65; lines 4-6, page 66; lines 22-25, page 72; lines 2-4, page 73; lines 23-25, page 75; lines 1-5, page 76, is directed to the respective element in the drawings of the present invention since each of them is not associated with any reference number in consistent with the reference number in the respective drawings of the present invention;

c) it is not understood how, during the erasing operation, the second negative voltage applied to the non-select row lines has an absolute value not larger than an absolute value of first negative voltage applied to the substrate or well as recited lines 18-23, page 11; lines 18-24, page 12; and lines 19-25, page 17 of the specification. Since from this disclosure, during the erasing operation, the absolute value of second negative voltage applied to the non-select row lines can be entitled to both first condition of "equal to" and second condition of "less than" the absolute value of first negative voltage applied to the substrate or well. However, the entire specification and the all drawings of the present invention only disclose the first condition of "equal to" which is-both the first negative voltage applied to the substrate or well and the second negative voltage applied to the non-select row lines are equal to –8V. Meanwhile, the second condition of "less than" is missing;

c) it is not understood how the negative voltage applied to the substrate or well as recited throughout the specification is generated. Figs. 1, 3-8 and 12-15 of the

present invention do not show any circuit for applying the desired negative voltage to the substrate or well of the non-volatile memory device;

d) the feature of the absolute value of the select voltage is equal to the absolute value of the negative voltage applied to the substrate or well as recited in claims 5-6 is not described in the specification as well as is seen in any drawings of the present invention. Only Table 2 in page 21 of the specification shows that, in the erase mode, the select voltage Vpp is 10V and the negative voltage applied to the substrate (well) Vneg is –8V.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

6. Claims 5-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There are no antecedent basis for 'the substrate or well" (last line).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 3-6 are, insofar as understood, rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al., 5,959,890.

Yamamoto et al., 5,959,890, discloses in Fig. 1 a non-volatile memory device

comprising:

memory cell array 400 which includes a plurality of memory cell blocks as shown in Fig. 9;

row selecting circuit 500, as shown in Fig. 3, comprising: word line driver circuits 520 for selecting/non-selecting word lines 401 according to the address signal ADD from row decoder 510 on a mode-by-mode basis from program mode, erase mode (see lines 18-19, column 4) and read mode (see line 8, column 9);

each of word line driver circuits 520 comprising, as shown in Fig. 4, signal generating circuit 521 (control voltage output means), for outputting a control voltage DSo responsive to the row decode address signals X and gate circuit 522;

select voltage output means from pad 1a in Fig. 1 for applying high power source potential Vcc to potential line 501 of gate 522, as shown in Fig. 7, for outputting a select voltage to a selected word line WL;

non-select voltage output means 300, as shown in Fig. 8, for applying a low voltage VL to potential line 502 of gate 522 for outputting a non-select voltage to a non-selected word line WL;

applied voltage select means SG as shown in Fig. 9;

substrate/well potential generating circuit 700;

wherein:

in the erase mode, a select positive voltage of 10V applied to the selected word line WL and a non-select negative voltage of –8V applied to the P-well PW (see lines 35-50, column 11).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakayama et al., 5,371,705, Onakado et al., 5,978,264, Yoshida, 5,267,209, Yamauchi et al., 6,512,692, and Yamauchi et al., JP2001357699.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (703) 308-4870. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-4021 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

phan trong

TRONG PHAN
PRIMARY EXAMINER

May 4, 2003